IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A method for fabricating an integrated circuit, comprising the steps of:

fabricating a portion of the integrated circuit, the portion comprising at least one active circuit area; [[and]]

fabricating a redistribution metal layer ~~at least partially during fabrication of the portion of the integrated circuit~~ over the at least one active circuit area;

depositing a polyimide layer over at least a portion of the redistribution metal layer; and

etching the polyimide layer to leave at least one portion of the redistribution metal layer open to receive at least one solder bump.

2. (Currently Amended) The method as set forth in Claim 1, wherein fabricating the redistribution metal layer comprises the step of:

fabricating at least one flat portion [[s]] of the redistribution metal layer ~~that are open~~ to receive [[a]] the at least one solder bump.

3. (Currently Amended) The method as set forth in Claim 1, wherein fabricating the portion of the integrated circuit and the redistribution metal layer comprises the steps of:

fabricating the active circuit area and an associated metal pad on a base substrate;

fabricating a vertical plug ~~; mounting the vertical plug~~ in electrical connection with the metal pad;

depositing an undoped silicon oxide layer on the active circuit area and on a portion of the metal pad;

depositing a phosphosilicate glass layer on the undoped silicon oxide layer;

depositing a silicon oxynitride layer over the phosphosilicate glass layer; and

depositing a flat metal layer over the silicon oxynitride layer and in electrical connection with the vertical plug.

4. (Currently Amended) The method as set forth in Claim 3, wherein ~~fabricating the redistribution metal layer further~~ depositing the polyimide layer and etching the polyimide layer comprise [[s]] the steps of:

depositing [[a]] the polyimide layer over at least one portion [[s]] of the flat metal layer and over at least one portion [[s]] of the silicon oxynitride layer; and

etching at least one portion [[s]] of the polyimide layer to leave at least one portion [[s]] of the flat metal layer open to receive [[a]] the at least one solder bump.

5. (Previously Presented) The method as set forth in Claim 1, wherein fabricating the portion of the integrated circuit and the redistribution metal layer comprises the steps of:

fabricating the active circuit area and an associated metal pad on a base substrate;

depositing an undoped silicon oxide layer on the active circuit area and on at least a portion of the metal pad;

depositing a phosphosilicate glass layer on the undoped silicon oxide layer;

depositing a metal layer over the phosphosilicate glass layer and in electrical connection with the metal pad; and

depositing a silicon oxynitride layer over at least some portions of the metal layer.

6. (Currently Amended) The method as set forth in Claim 5, wherein ~~fabricating the redistribution metal layer further~~ depositing the polyimide layer comprises the step of:

depositing the polyimide layer over at least a portion of the silicon oxynitride layer ~~leaving portions of the metal layer open to receive a solder bump~~.

7. (Previously Presented) The method as set forth in Claim 5, wherein depositing the silicon oxynitride layer comprises the step of:

depositing a silicon oxynitride layer over all portions of the metal layer.

8. (Currently Amended) The method as set forth in Claim 7, ~~wherein fabricating the redistribution metal layer~~ further comprising [[es]] the step of:

etching the silicon oxynitride layer to a pattern that leaves at least one portion [[s]] of the metal layer uncovered to receive [[a]] the at least one solder bump.

9. (Currently Amended) The method as set forth in Claim 5, wherein ~~fabricating the redistribution metal layer further~~ depositing the polyimide layer and etching the polyimide layer comprise [[s]] the steps of:

depositing [[a]] the polyimide layer over at least one portion [[s]] of the metal layer and over at least one portion [[s]] of the silicon oxynitride layer; and

etching at least one portion [[s]] of the polyimide layer to leave at least one portion [[s]] of the flat metal layer open to receive [[a]] the at least one solder bump.

10. (Previously Presented) The method as set forth in Claim 1, wherein fabricating the redistribution metal layer comprises the step of:

fabricating the redistribution metal layer using a last metal layer that is used to fabricate the active circuit area of the integrated circuit.

11. (Currently Amended) An integrated circuit, comprising:

a portion comprising at least one active circuit area; [[and]]

a redistribution metal layer fabricated ~~at least partially during fabrication of the portion of the integrated circuit~~ over the at least one active circuit area; and

a polyimide layer deposited over at least a portion of the redistribution metal layer;

wherein the polyimide layer is etched to leave at least one portion of the redistribution metal layer open to receive at least one solder bump.

12. (Currently Amended) The integrated circuit as set forth in Claim 11, wherein at least one flat portion [[s]] of the redistribution metal layer in the integrated circuit ~~are open to~~ receives [[a]] the at least one solder bump.

13. (Previously Presented) The integrated circuit as set forth in Claim 11, wherein the portion of the integrated circuit and the redistribution metal layer comprise:

the active circuit area and an associated metal pad on a base substrate;

a vertical plug mounted on and electrically connected to the metal pad;

an undoped silicon oxide layer deposited on the active circuit area and on a portion of the metal pad;

a phosphosilicate glass layer deposited on the undoped silicon oxide layer;

a silicon oxynitride layer deposited on the phosphosilicate glass layer; and

a flat metal layer deposited over the silicon oxynitride layer;

wherein the flat metal layer is electrically connected to the vertical plug.

14. (Currently Amended) The integrated circuit as set forth in Claim 13, wherein the ~~redistribution metal layer further~~ polyimide layer comprises:

a polyimide layer deposited over at least one portion [[s]] of the flat metal layer and over at least one portion [[s]] of the silicon oxynitride layer [[;]]

~~wherein the polyimide layer is etched to leave portions of the flat metal layer open to receive a solder bump~~.

15. (Previously Presented) The integrated circuit as set forth in Claim 11, wherein the portion of the integrated circuit and the redistribution metal layer comprise:

the active circuit area and an associated metal pad on a base substrate;

an undoped silicon oxide layer deposited on the active circuit area and on at least a portion of the metal pad;

a phosphosilicate glass layer deposited on the undoped silicon oxide layer;

a metal layer deposited over the phosphosilicate glass layer, wherein the metal layer is electrically connected to the metal pad; and

a silicon oxynitride layer deposited over at least some portions of the metal layer.

16. (Currently Amended) The integrated circuit as set forth in Claim 15, wherein at least one flat portion [[s]] of the metal layer [[are]] is open to receive [[a]] the at least one solder bump.

17. (Currently Amended) The integrated circuit as set forth in Claim 15, wherein the silicon oxynitride layer comprises:

a silicon oxynitride layer deposited over all portions of the metal layer and etched to a pattern that leaves at least one portion [[s]] of the metal layer uncovered to receive [[a]] the at least one solder bump.

18. (Previously Presented) The integrated circuit as set forth in Claim 15, wherein the ~~redistribution metal layer further~~ polyimide layer comprises:

a polyimide layer deposited over at least one portion [[s]] of the metal layer and over at least one portion [[s]] of the silicon oxynitride layer [[;]]

~~wherein portions of the metal layer are open to receive a solder bump~~.

19. (Previously Presented) The integrated circuit as set forth in Claim 11, wherein the redistribution metal layer comprises:

a redistribution metal layer fabricated using a last metal layer that is used to fabricate the active circuit area of the integrated circuit.

20. (Previously Presented) The integrated circuit as set forth in Claim 12, further comprising:

a solder bump attached to the portions of the redistribution metal layer that are open to receive a solder bump.

21. (Previously Presented) The integrated circuit as set forth in Claim 14, further comprising:

a solder bump attached to the portions of the flat metal layer that are open to receive a solder bump.

22. (Previously Presented) The integrated circuit as set forth in Claim 16, further comprising:

a solder bump attached to the portions of the flat metal layer that are open to receive a solder bump.

Claims 23-30 (Cancelled).